

I CLAIM:

1. A deposition method comprising:
providing a substrate disposed within a chamber, wherein the substrate comprises a first surface having a first surface morphology and a second surface having a second surface morphology different from the first surface morphology;
introducing trisilane to the chamber under chemical vapor deposition conditions; and
depositing a Si-containing film onto the substrate over both of the first surface and the second surface.
2. The deposition method of Claim 1, wherein the first surface morphology is single crystalline.
3. The deposition method of Claim 2, wherein the second surface morphology is amorphous, polycrystalline or a mixture of amorphous and crystalline material.
4. The deposition method of Claim 2, further comprising introducing a germanium source to the chamber simultaneously with the trisilane, thereby depositing a SiGe film as the Si-containing film.
5. The deposition method of Claim 4, wherein the SiGe film comprises from about 0.1 atomic % to about 80 atomic % germanium.
6. The deposition method of Claim 1, wherein the first surface comprises a semiconductor material and the second surface comprises a dielectric material.
7. The deposition method of Claim 6, wherein the semiconductor material comprises silicon and a dopant selected from the group consisting of arsenic, boron, indium, phosphorous, and antimony.
8. The deposition method of Claim 6, wherein the dielectric material comprises a material selected from the group consisting of silicon dioxide, silicon nitride, metal oxide and metal silicate.
9. The deposition method of Claim 1, wherein the Si-containing film is a silicon buffer layer having a thickness of about 500 Å or less.

10. The deposition method of Claim 9, further comprising introducing a germanium source and a silicon source to the chamber to thereby deposit a SiGe film onto the buffer layer.

11. The deposition method of Claim 10, wherein the silicon source comprises trisilane.

12. The deposition method of Claim 1, wherein at least a portion of the first surface is non-coplanar with at least a portion of the second surface.

13. The deposition method of Claim 12, wherein the Si-containing film has a first thickness T_1 over the first surface and a second thickness T_2 over the second surface such that $T_1:T_2$ is in the range of about 10:1 to about 1:10.

14. The deposition method of Claim 13, wherein the chemical vapor deposition conditions comprise a temperature in the range of about 400°C to about 750°C.

15. The deposition method of Claim 13, wherein the Si-containing film has a first thickness T_1 over the first surface and a second thickness T_2 over the second surface such that $T_1:T_2$ is in the range of about 2:1 to about 1:2.

16. The deposition method of Claim 15, wherein the Si-containing film has a first thickness T_1 over the first surface and a second thickness T_2 over the second surface such that $T_1:T_2$ is in the range of about 1.3:1 to about 1:1.3.

17. The deposition method of Claim 1, further comprising introducing a dopant precursor to the chamber, thereby depositing an *in situ* doped Si-containing film as the Si-containing film.

18. The deposition method of Claim 1, wherein the Si-containing film comprises a crystalline morphology over the first surface and a non-crystalline morphology over the second surface.

19. A high-rate deposition method comprising:

delivering trisilane to a mixed substrate surface under chemical vapor deposition conditions, at a delivery rate of at least about 0.001 milligrams per minute per square centimeter of the mixed substrate surface, and

depositing a silicon-containing material onto the mixed substrate surface at a rate of about 10 Å per minute or greater.

20. The high-rate deposition method of Claim 19, wherein the mixed substrate surface comprises an exposed conductive material and an exposed dielectric material.

21. The high-rate deposition method of Claim 20, wherein the conductive material comprises a crystalline semiconductor.

22. The high-rate deposition method of Claim 21, wherein the crystalline semiconductor comprises a dopant selected from the group consisting of boron, gallium, indium, phosphorus, arsenic and antimony.

23. The high-rate deposition method of Claim 19, further comprising delivering a germanium source to the mixed substrate surface to thereby deposit a SiGe material as the silicon-containing material.

24. The high-rate deposition method of Claim 23, wherein the delivering of the germanium source to the mixed substrate surface is conducted at a delivery rate of at least about 0.001 milligrams per minute per square centimeter of the mixed substrate surface.

25. A method for making a base structure for a heterojunction bipolar transistor (HBT), comprising:

providing a substrate surface comprising an active area and an insulator; and

supplying trisilane to the substrate surface under conditions effective to deposit a Si-containing film onto the substrate directly onto each of the active area and the insulator.

26. The method of Claim 25, wherein the Si-containing film has a first thickness T_1 over the active area and a second thickness T_2 over the insulator such that $T_1:T_2$ is in the range of about 2:1 to about 1:2.

27. The method of Claim 26, wherein the Si-containing film has a first thickness T_1 over the active area and a second thickness T_2 over the insulator such that $T_1:T_2$ is in the range of about 1.3:1 to about 1:1.3.

28. The method of Claim 25, further comprising supplying a silicon source under conditions effective to deposit a cap layer onto the Si-containing film.

29. The method of Claim 25, further comprising supplying a germanium source to the substrate surface simultaneously with the trisilane under conditions effective to deposit a SiGe film as the Si-containing film.

30. The method of Claim 25, wherein the Si-containing film is a nucleation layer having a thickness in the range of about 10 Å to about 500 Å.

31. The method of Claim 25, wherein the Si-containing film is a nucleation layer having a thickness in the range of about 50 Å to about 300 Å.

32. The method of Claim 30, further comprising supplying a mixture comprising trisilane and a germanium source to the nucleation layer under conditions effective to deposit a SiGe film onto the nucleation layer.

33. A method for reducing the number of steps in a semiconductor device manufacturing process, comprising:

identifying a semiconductor device manufacturing process that comprises (a) depositing a first silicon-containing film onto a non-epitaxial surface using a first silicon source and, in a separate step, (b) depositing a second silicon-containing film onto a single-crystal surface using a second silicon source; wherein the first silicon source and the second silicon source are each individually selected from the group consisting of silane, disilane, dichlorosilane, trichlorosilane and silicon tetrachloride; and

modifying the semiconductor device manufacturing process by replacing the first silicon source and the second silicon source with trisilane and simultaneously depositing a third silicon-containing film onto the epitaxial surface and the non-epitaxial surface in the same step.

34. The method of Claim 33, wherein the semiconductor device manufacturing process comprises a masking step for opening a window onto the epitaxial surface after depositing the first silicon-containing film and prior to depositing the second silicon-containing film.

35. The method of Claim 34, wherein the modifying of the semiconductor device manufacturing process comprises eliminating the masking step.